

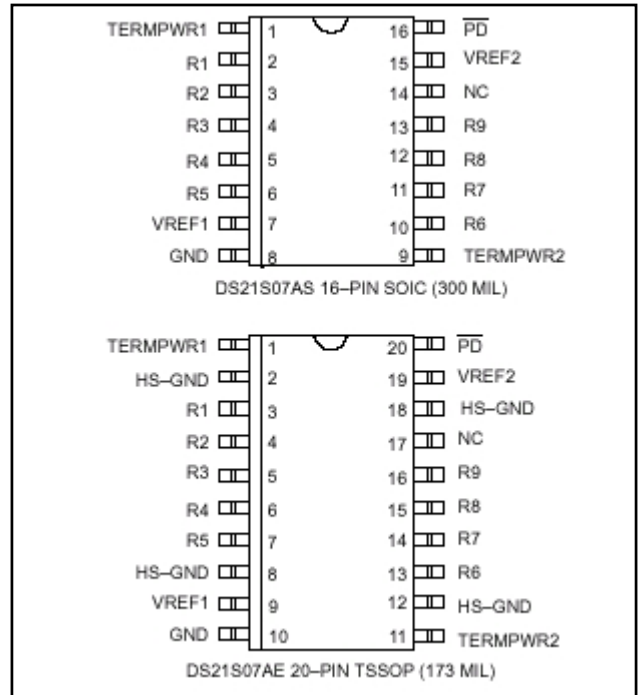
GENERAL DESCRIPTION

Fast SCSI and Ultra SCSI require the use of active terminations at both ends of every cable segment in a SCSI system with single-ended drivers and receivers. The DS21S07A SCSI terminator, which is fully compliant with these standards, enables the designer to gain the benefits of active termination: greater immunity to voltage drops on the TERMPWR (TERMination PoWeR) line, enhanced high-level noise immunity, intrinsic TERMPWR decoupling, and very low quiescent current consumption. The DS21S07A integrates a regulator and nine precise switched 110Ω termination resistors into a monolithic IC. The DS21S07A can be electrically isolated from the SCSI bus without physical removal from the SCSI device.

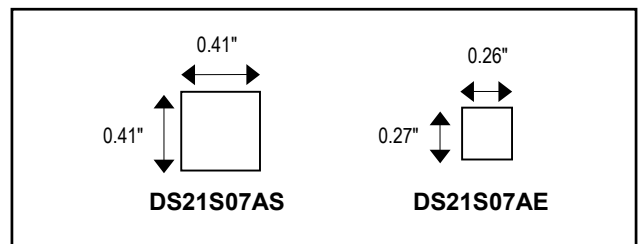
FEATURES

- Fully Compliant with SCSI-1, Fast SCSI, and Ultra SCSI
- Backward Compatible to the DS2107 and DS2107A
- Provides Active Termination for Nine Signal Lines
- Laser-Trimmed 110Ω Termination Resistors Have 2% Tolerance
- Low Drop-Out Voltage Regulator
- Power-Down Mode Isolates Termination Resistors from the Bus
- SCSI Bus Hot Plug Compatible
- Fully Supports Actively Negated SCSI Signals
- On-Board Thermal Shutdown Circuitry
- 16-Pin Plastic SO (DS21S07AS) and 20-Pin Plastic TSSOP (Thin Shrink Small Outline Package) (DS21S07AE)

PIN CONFIGURATIONS



ACTUAL FOOTPRINT SIZE



ORDERING INFORMATION

PART	VOLTAGE (V)	PIN-PACKAGE	TOP MARK
DS21S07AS	5	16SO	DS21T07S
DS21S07AS+	5	16SO	DS21T07S
DS21S07AS/T&R	5	16SO	DS21T07S
DS21S07AS+T&R	5	16SO	DS21T07S
DS21S07AE	5	20TSSOP	DS21T07E
DS21S07AE/T&R	5	20TSSOP	DS21T07E

+ Denotes lead-free package. The top mark includes a "+" on lead-free packages.
Note: All devices are specified over the 0°C to +70°C operating temperature range.

FUNCTIONAL DESCRIPTION

The DS21S07A consists of a bandgap reference, buffer amplifier, and nine termination resistors (Figure 1). The bandgap reference circuit produces a precise 2.55V level that is fed to a buffer amplifier. The buffer produces a 2.85V level and can source at least 24mA into each of the termination resistors when the signal line is low (active). When the driver for a given signal line turns off, the terminator pulls the signal line to 2.85V (quiescent state). To handle actively negated SCSI signals, the buffer can sink at least 200mA, and VREF will move less than 60mV. When all lines settle in the quiescent state, the regulator consumes about 2.5mA. When the DS21S07A is put into power-down mode by bringing $\overline{\text{PD}}$ low, the power-down circuitry turns off the transistors on each signal line. This isolates the DS21S07A from the signal lines and effectively removes it from the circuit. The power-down pin ($\overline{\text{PD}}$) has an internal 50k Ω pullup resistor. To place the DS21S07A into an active state, the $\overline{\text{PD}}$ pin should be left open circuited. When installed on disk drives or RAID system components, the DS21S07A will not affect the SCSI bus during a hot plug operation.

To ensure proper operation, both the TERMPWR1 and TERMPWR2 pins must be connected to the SCSI bus TERMPWR line and both the VREF1 and VREF2 pins must be tied together externally. Each DS21S07A requires a 4.7 μF capacitor connected between the VREF pins and ground. Figure 2 details a typical SCSI bus configuration. In an 8-bit-wide SCSI bus arrangement ("A" Cable), two DS21S07A's would be needed at each end of the SCSI cable to terminate the 18 active signal lines. In a 16-bit-wide SCSI bus arrangement ("P" Cable), three DS21S07A's would be needed at each end of the SCSI cable to terminate the 27 active signal lines.

Figure 1. DS21S087A Block Diagram

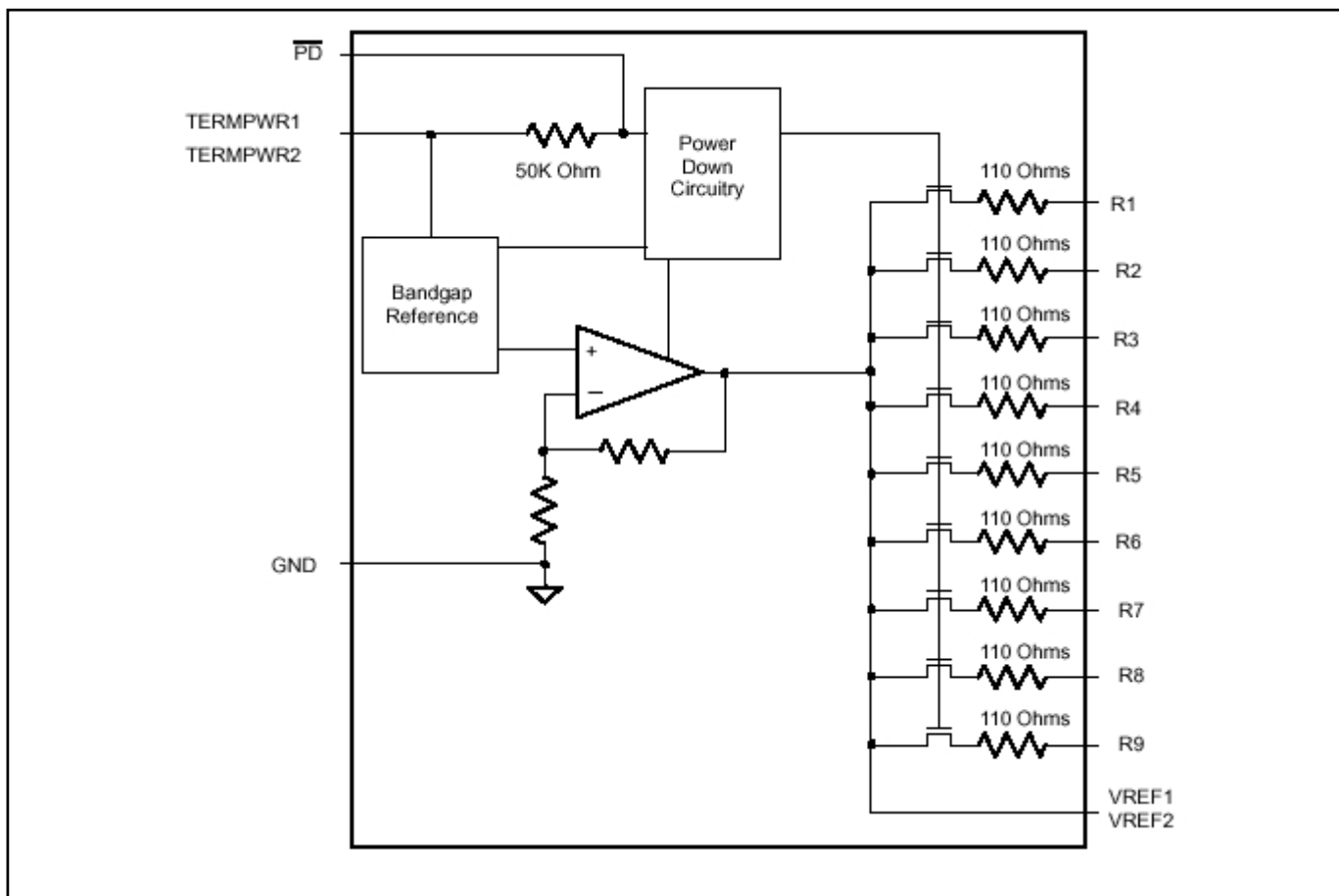
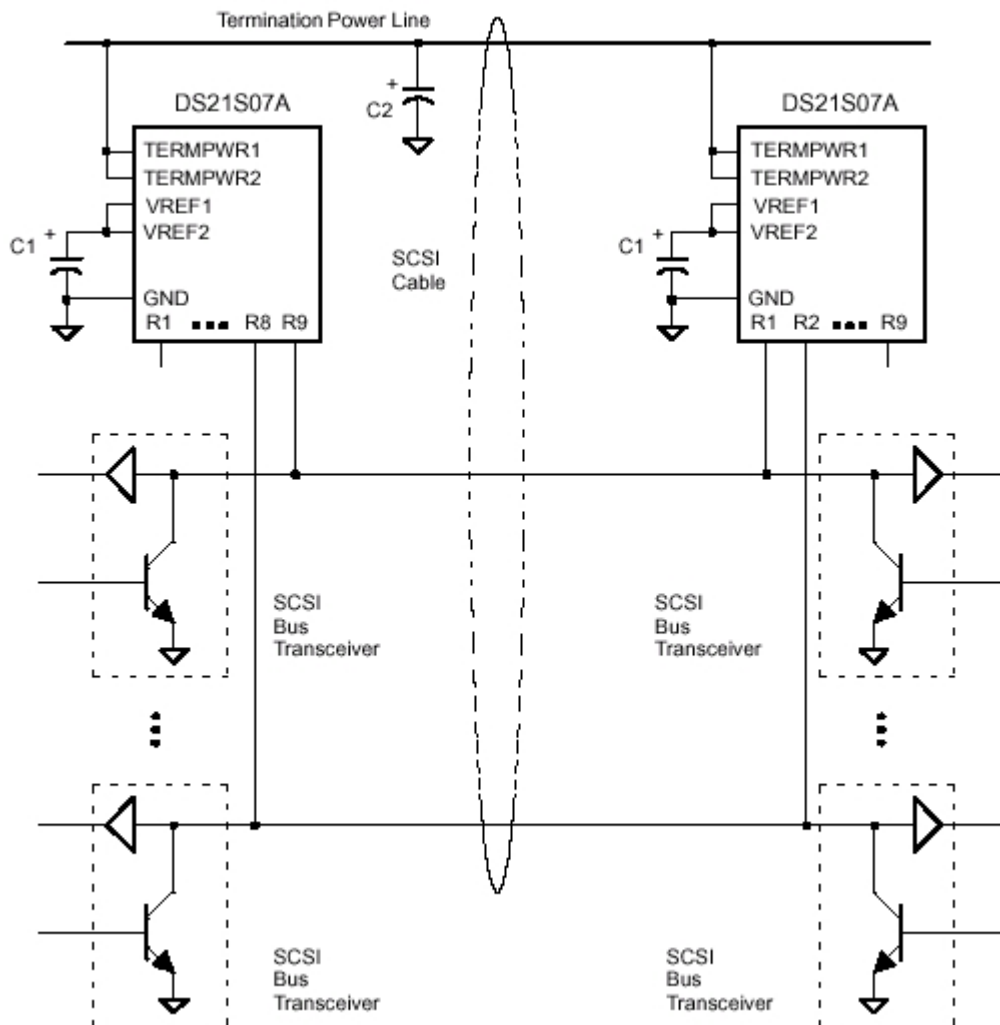


Figure 2. Typical Differential SCSI Bus Configuration


NOTE 1: C1 = 4.7 μ F TANTALUM CAPACITOR; C2 = 2.2 μ F TANTALUM OR 4.7 μ F ALUMINUM CAPACITOR.

NOTE 2: IF THE DS21S07A IS TO BE EMBEDDED INTO A PERIPHERAL THAT WILL ACT AS A TARGET ON A SCSI BUS, IT IS RECOMMENDED THAT TERMPWR BE DERIVED FROM THE SCSI CABLE, NOT GENERATED LOCALLY. IN THIS CONFIGURATION, IF A POWER FAILURE OCCURS IN THE PERIPHERAL, IT WILL NOT AFFECT THE BUS.

NOTE 3: A HIGH-FREQUENCY BYPASS CAPACITOR (0.1 μ F RECOMMENDED) CAN BE ADDED IN PARALLEL TO C1 FOR APPLICATIONS USING FAST RISE/FALL TIME DRIVERS.

Table 1. Pin Description

PIN		NAME	FUNCTION
TSSOP	SO		
1	1	TERMPWR1	Termination Power 1. Should be connected to the SCSI TERMPWR line. Must be decoupled with either a 2.2 μ F capacitor or 4.7 μ F capacitor. See Figure 2.
2, 8, 12, 18	—	HS-GND	Heat Sink Ground. Internally connected to the mounting pad. Should be either grounded or electrically isolated from other circuitry.
3–7, 13–16	2–6, 10–13	R1–R9	Signal Termination 1–9. 110 Ω termination.
9	7	VREF1	Reference Voltage 1. Must be externally connected directly to the VREF2 pin. Must be decoupled with a 4.7 μ F capacitor as shown in Figure 2.
10	8	GND	Ground. 0V, signal ground.
11	9	TERMPWR2	Termination Power 2. Should be connected to the SCSI TERMPWR line. Must be decoupled with either a 2.2 μ F capacitor or 4.7 μ F capacitor. See Figure 2.
17	14	NC	No Connection. Do not connect any signal to this pin.
19	15	VREF2	Reference Voltage 2. Must be externally connected directly to the VREF1 pin. Must be decoupled with a 4.7 μ F capacitor as shown in Figure 2.
20	16	$\overline{\text{PD}}$	Active-Low Power-Down. When tied low, the DS21S07A enters a power-down mode. Contains an internal 50k Ω pullup resistor. Strap low to deactivate the DS21S07A; leave open circuited to activate the DS21S07A

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground.....	-1.0V to +7.0V
Operating Temperature Range.....	0°C to +70°C
Storage Temperature Range.....	-55°C to +125°C
Soldering Temperature.....	See IPC/JEDEC J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

RECOMMENDED OPERATING CONDITIONS(T_A = 0°C to +70°C)

PARAMETER	SYM	MIN	TYP	MAX	UNITS	NOTES
TERMPWR Voltage	V _{TP}	4.00		5.50	V	
$\overline{\text{PD}}$ Active	V _{PDA}	-0.3		+0.8	V	
$\overline{\text{PD}}$ Inactive	V _{PDI}	2.0		V _{TP} + 0.3	V	

DC CHARACTERISTICS(T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TERMPWR Current	I _{TP}			250	mA	1, 3
			2.5	5	mA	1, 4
Power-Down Current	I _{PD}		100	150	μA	1, 2, 5
Termination Resistance	R _{TERM}	108	110	112	Ω	1, 2
Die Thermal Shutdown	T _{SD}	150			°C	1, 6
Power-Down Termination Capacitance	C _{PD}		3.0	5.0	pF	1, 2, 5, 6
Input Leakage High	I _{IH}	-1.0			μA	1, 8
Input Leakage Low	I _{IL}			1.0	μA	1, 7

REGULATOR CHARACTERISTICS(T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Voltage	V _{REF}	2.79	2.85	2.93	V	1, 2
Drop-Out Voltage	V _{DROP}		0.50	0.75	V	3, 6
Line Regulation	L _{REG}		1.0	2.0	%	1, 4
Load Regulation	L _{OREG}		1.3	3.0	%	1, 3
Current Limit	I _{LIM}		350		mA	1
Sink Current	I _{SINK}	200			mA	1

NOTES:

- 1) $4.00V < \text{TERMPWR} < 5.50V$.
- 2) $0.0V < \text{signal lines} < \text{TERMPWR}$.
- 3) All signal lines = $0V$.
- 4) All signal lines open.
- 5) $\overline{\text{PD}} = 0V$.
- 6) Guaranteed by design; not production tested.
- 7) R1 to R9 only.
- 8) R1 to R9 and $\overline{\text{PD}}$.

PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/DallasPackInfo.)

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	NEW DRAWING	5/18	J.W.
B	INC. ECN NO. 8680		

LTR	MIN	MAX											
A	IN. MM	0.094 2.39	0.105 2.67										
A1	IN. MM	0.004 0.102	0.012 0.30										
A2	IN. MM	0.089 2.26	0.095 2.41										
b	IN. MM	0.013 0.33	0.020 0.51										
C	IN. MM	0.009 0.229	0.013 0.33	16 PIN MIN	18 PIN MIN	20 PIN MIN	24 PIN MIN	28 PIN MIN	16 PIN MAX	18 PIN MAX	20 PIN MAX	24 PIN MAX	28 PIN MAX
D	IN. MM	→		0.398 10.11	0.412 10.46	0.448 11.38	0.462 11.73	0.498 12.65	0.511 12.99	0.598 15.19	0.612 15.54	0.698 17.73	0.712 18.08
e	IN. MM	.050 BSC											
E1	IN. MM	0.290 7.37	0.300 7.62										
H	IN. MM	0.398 10.11	0.416 10.57										
L	IN. MM	0.016 0.40	0.040 1.02										
θ		0°	8°										

THE CHAMFER ON THE BODY IS OPTIONAL.
 IF IT IS NOT PRESENT, A TERMINAL 1 IDENTIFIER
 MUST BE POSITIONED SO THAT 1/2 OR MORE OF
 IT'S AREA IS CONTAINED IN THE HATCHED ZONE.

SIGNATURE		DATE				
DOC. CONTROL: J.WILKINS		5/94				
ENGR. MGR: B.W.MCARTY		5/94	TITLE PACKAGE OUTLINE .300" SOIC 16,18,20,24&28 LD.			
MFG. ENGR: C.M.SELLS		5/94				
CHECKED BY: C.M.SELLS		5/94				
DRAWN BY: M.W.C.		5/94	SIZE A	FSCM NO.	PART NO. 56-G4009-001	REV B
DO NOT SCALE DWG.			SCALE N/A		SHEET 1 OF 1	

PACKAGE INFORMATION (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/DallasPackInfo.)

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	NEW DRAWING	12/92	K.D.
B	INC. ECN NO. 6791		

1

NOTES:

1. DIMENSION "D" INCLUDES MOLD MISSMATCH, FLASH, AND PROTRUSIONS.

SEE DETAIL A

DIM	MIN	MAX
A	—	1.10
A1	0.05	—
A2	0.75	1.05
c	0.09	0.18
phi	0°	8°
L	0.50	0.70
e1	0.65	BSC
B	0.18	0.30
D	6.40	6.90
E	4.40	NOM
G	0.25	REF
H	6.25	6.55

DETAIL A

DIMENSIONS ARE IN MILLIMETERS

SIGNATURE		DATE			
DOC. CONTROL:	J.WILKINS	6/92			
ENGR. MGR:	J.HUNDT	6/92	TITLE		
MFG. ENGR:	B.W.M.	6/92			MARKETING OUTLINE, 20 LD. TSSOP, 4.4 MM BODY
CHECKED BY:	B.W.M.	6/92	SIZE	FSCM NO	
DRAWN BY:	M.W.C.	6/92	A		
DO NOT SCALE DWG.		SCALE	N/A	PART NO.	56-G2010-000
				REV	B
				SHEET	1 OF 1

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